WHAT IS CLAIMED IS:

1. A digital line build out circuit comprising:

a memory storing a plurality of digitized waveforms;

a selection circuit, coupled to said memory, to select certain ones of said waveforms corresponding to an anticipated amount of signal degradation over a transmission line; and

a digital to analog converter to convert said certain ones of said waveforms into analog waveforms for transmission.

2. The circuit of claim 1 further comprising:

a counter having an output coupled to inputs of said memory for sequentially selecting multiple samples of said digitized waveforms during a period.

3. The circuit of claim 1 wherein said memory comprises a ROM.

4. The circuit of claim 1 further comprising:

a combining circuit, coupled between said memory and said digital to analog converter, to combine a portion of a current digitized waveform with a portion of at least one previous digitized waveform.

5. The circuit of claim 4 wherein said combining circuit includes at least one delay element for delaying an output of said memory for said previous digitized waveform for combination with said current digitized waveform.

6. The circuit of claim 5 wherein said delay element delays a data bit, and further comprising a circuit for gating a portion of said digitized waveform from said memory based on a value of said data bit.

7. The circuit of claim 4 wherein said combining circuit combines portion of a current waveform with portions of three previous waveforms.

8. A digital line build out circuit comprising:

a memory storing a plurality of digitized waveforms;

a selection circuit, coupled to said memory, to select certain ones of said waveforms corresponding to an anticipated amount of signal degradation over a transmission line;

a digital to analog converter to convert said certain ones of said waveforms into analog waveforms for transmission;

a counter having an output coupled to inputs of said memory for sequentially selecting multiple samples of said digitized waveforms during a period; and

a combining circuit, coupled between said memory and said digital to analog converter, to combine a portion of a current digitized waveform with a portion of at least one previous digitized waveform.

9. A digital line build out circuit comprising:

a memory storing a plurality of digitized waveforms corresponding to different anticipated amounts of signal degradation over a transmission line, each of said digitized waveforms having a plurality of separately addressable portions;

a data line coupled to a plurality of serial delay elements;

a plurality of gating circuits having a first input coupled to one of said data line and an output of each of said delay elements, and a second input coupled to an output of said memory for one of said separately addressable portions;

a combining circuit having inputs coupled to outputs of said gating circuits for combining multiple ones of said separately addressable portions;

a digital to analog converter coupled to an output of said combining circuit;

a configuration input, coupled to said memory, for selecting a desired one of said plurality of digitized waveforms; and

a counter, coupled to said memory, for sequentially selecting a plurality of digitized values for said separately addressable portions.

10. The circuit of claim 9 wherein said memory is a ROM.

11. The circuit of claim 9 wherein said memory comprises a plurality of memories.

12. The circuit of claim 9 where said gating circuits comprise a multiplier circuits.

13. The circuit of claim 9 wherein said gating circuits comprise selector circuits.